IN THE CLAIMS

1. (Currently amended) An adder comprising:

a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and

a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being separate and distinct from the primary carry-output signal, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder;

wherein the adder comprises an n-bit adder and the primary carry-output signal comprises a primary carry-output signal c_{n-1} of the n-bit adder.

2. (Original) The adder of claim 1 wherein the adder comprises an n-bit adder and the sum output signal comprises a final sum bit s_{n-1} of the n-bit adder.

3. (Canceled)

4. (Original) The adder of claim 1 wherein the flag generation circuit does not require the primary carry-output signal to generate the overflow flag for the adder.

5. (Previously presented) An adder comprising:

a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and

a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder;

wherein the adder comprises an n-bit adder and the flag generation circuit generates an overflow flag OVF as:

$$OVF = c_{n-2}\bar{t}_{n-1} + g_{n-1}\bar{c}_{n-2},$$

where c_{n-2} is an n-2 carry signal of the adder, t_{n-1} is an n-1 transmit signal of the adder, and g_{n-1} is an n-1 generate signal of the adder, such that the generation of the overflow flag OVF does not require the use of a primary carry-output signal c_{n-1} of the adder.

6. (Previously presented) An adder comprising:

a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and

a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder;

wherein the flag generation circuit comprises a multiplexer which selects one of a plurality of input signals for propagation to its output as the overflow flag based at least in part on a signal associated with the signal line of at least one of the computational stages.

7. (Previously presented) An adder comprising:

a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and

a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder;

wherein the flag generation circuit comprises a 2-to-1 multiplexer having a first input having a first signal applied thereto, a second input having a second signal applied thereto, an output corresponding to the overflow flag, and a select signal input for selecting one of the first signal and the second signal for propagation to the output as the overflow flag.

8. (Original) The adder of claim 7 wherein the adder comprises an n-bit adder and the multiplexer receives as the first input a transmit signal t_{n-1}, receives as the second input a generate signal $\overline{g}_{n-1}$, receives as the select signal a carry signal c_{n-2}, and depending on the value of the select signal, the multiplexer selects either the transmit signal t_{n-1} or the generate signal $\overline{g}_{n-1}$ for propagation in inverted form to its output as the overflow flag.

9. (Original) The adder of claim 1 wherein the adder comprises a prefix tree adder having a plurality of prefix trees, each associated with one of the bit positions of the adder and including one or more of the computation stages.

10. (Original) The adder of claim 1 wherein the adder comprises a carry-lookahead adder.

11. (Original) The adder of claim 1 wherein the adder comprises a carry-skip adder.

12. (Original) The adder of claim 1 wherein the adder comprises a carry-ripple adder.

13. (Original) The adder of claim 1 wherein the adder comprises a carry-save adder.

14. (Original) The adder of claim 1 wherein the adder comprises a radix-2 adder.

15. (Original) The adder of claim 1 wherein the adder comprises a non-radix-2 adder.

16. (Currently amended) An integrated circuit comprising:

at least one adder, the adder comprising: (i) a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and (ii) a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being separate and distinct from the primary carry-output signal, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder;

wherein the adder comprises an n-bit adder and the primary carry-output signal comprises a primary carry-output signal c_{n-1} of the n-bit adder.

17. (Currently amended) A method for performing a computational operation in an adder, the method comprising the steps of:

providing a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and

generating an overflow flag for the adder using at least one signal associated with at least one of the computational stages, the overflow flag being separate and distinct from the primary carry-output signal, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder;

wherein the adder comprises an n-bit adder and the primary carry-output signal comprises a primary carry-output signal c_{n-1} of the n-bit adder.